REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Drawing updated to reflect current requirements. – gt	02-07-11	R. Monnin

REV																				
SHEET																				
REV	A	A	A	A	A	A	A	A	A											
SHEET	15	16	17	18	19	20	21	22	23											

REV STATUS	REV	A	A	A	A	A	A	A	A	A	A	A	A	A	A	A
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

PMIC N/A

PREPARED BY
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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS

AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
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APPROVED BY
Raymond Monnin

DRAWING APPROVAL DATE
99-10-18

REVISION LEVEL
A

MICROCIRCUIT, LINEAR, 12-BIT ANALOG-TO-DIGITAL CONVERTER WITH MICROPROCESSOR INTERFACE, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-99582**

SHEET 1 OF 23

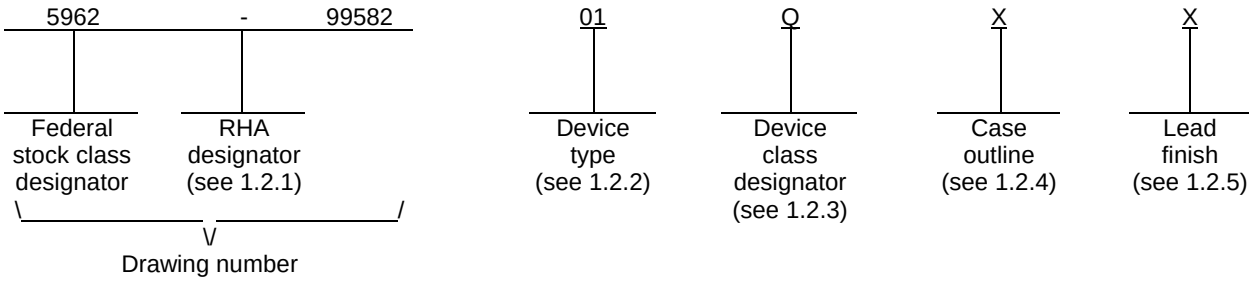
DSCC FORM 2233
APR 97

5962-E393-02

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	774T	12-bit A/D converter with microprocessor interface

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	CDIP2-T28	28	Dual-in-line

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/

V_{CC} to digital common	0 V to +16.5 V
V_{EE} to digital common	0 V to -16.5 V
V_{LOGIC} to digital common	0 V to +7 V
Analog common to digital common	±1 V
Control inputs (CE, $\overline{CS}$, A_0, 12/$\overline{8}$, R/$\overline{C}$) to digital common	-0.5 V to V_{LOGIC} +0.5 V
Analog inputs (REFIN, BIPOFF, 10 V_{IN}) to analog common	±16.5 V
20 V_{IN} to analog common	±24 V
REFOUT	Indefinite short to common, momentary short to V_{CC}
Power dissipation (at T_A = 75°C) (P_D)	1.29 W 2/
Lead temperature (soldering, 10 seconds)	+275°C
Storage temperature	-65°C to 150°C
Thermal resistance, junction-to-ambient (θ_{JA})	77°C/W
Thermal resistance, junction-to-case (θ_{JC})	18°C/W
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

$+V_{SUPPLY}$	+15 V
$-V_{SUPPLY}$	-15 V
V_{LOGIC}	+5 V
V_{REF}	+10 V
Analog input voltage, 10V_{IN}	±5 V or 0 to +10 V
Analog input voltage, 20 V_{IN}	3/
Logic level low (V_{IL})	0 V to 0.8 V
Logic level high (V_{IH})	2.0 V to +5 V
Ambient operating temperature range (T_A)	-55°C to 125°C

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Power dissipation derating factor at T_A > +75°C is 12.9 mW/°C.
3/ The 20 V input range (pin 14) is functional but performance is not guaranteed. Table I is guaranteed for only the 0 V to +10 V and ±5 V ranges (pin 13). The 20 V input (pin 14) should be left open. The 20 V input is tied to the 10 V input through 5 kΩ and will effect circuit operation if connected to any potential.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Block diagram. The block diagram shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-PRF-38535, appendix A.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Bipolar input voltage range 2/	V_{IN}		1, 2, 3	01	-5	+5	V
					-10	+10	
Unipolar input voltage range 2/	V_{IN}		1, 2, 3	01	0	+10	V
					0	+20	
Input voltage (CE, $\overline{CS}$, R/$\overline{C}$, A_O, 12/$\overline{8}$)	V_{IH}	Logic "1"	1, 2, 3	01	+2.0		V
	V_{IL}	Logic "0"	1, 2, 3			+0.8	
Power supply current from V_{CC}	I_{CC}		1, 2, 3	01		15	mA
Power supply current from V_{EE}	I_{EE}		1	01		28	mA
			2, 3			30	
Power supply current from V_{LOGIC}	I_{LOG}		1	01		15	mA
			2, 3			17	
Power dissipation 2/ 3/	P_D	Calculated worst case of 2 conditions	1	01		720	mW
			2, 3			760	
Input low current	I_{IL}	V_{LOGIC} = 5.5 V, V_{IN}(LOGIC) = 0.0 V	1, 2, 3	01	-5	5	µA

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input high current	I_{IH}	V_{LOGIC} = 5.5 V, V_{IN}(LOGIC) = 2.0 V	1, 2, 3	01	-5	5	µA
		V_{IN}(LOGIC) = 5.5 V	1, 2, 3	01	-5	5	
High impedance state output current	I_{ZL}	V_{LOGIC} = 5.5 V, V_{IN} = 11.0 V min, Output code = 111111111111, Set R/$\overline{C}$ = Logic "0" Output bits 1 thru 12 measured separately, V_{OUT} = 0.0 V all bits	1, 2, 3	01	-5	5	µA
High impedance state output current	I_{ZH}	V_{LOGIC} = 5.5 V, V_{IN} = -1.0 V max, Output code = 000000000000, Set R/$\overline{C}$ = Logic "0" Output bits 1 thru 12 measured separately, V_{OUT} = 5.5 V all bits	1, 2, 3	01	-5	5	µA
Output logic voltage levels	V_{OL}	V_{LOGIC} = 4.5 V, Output code = 000000000000, Measure output bits 1 thru 12 & STS, I_L = 1.6 mA	1, 2, 3	01		0.5	V
	V_{OH}	V_{LOGIC} = 4.5 V, Output code = 111111111111, Measure bits 1 thru 12, I_L = -0.5 mA	1, 2, 3	01	2.4		V
Reference voltage	V_{REF}	Output code = 000000000000, Bipolar VFSR = 20 V, I_L = 2.0 mA	1	01	9.970	10.030	V
			2,3		9.950	10.050	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Power supply sensitivity to V_{CC}	$+PSS_1$	13.5 V ≤ V_{CC} ≤ 16.5 V, Output transition = 11111111111X - 00000000000X 4/	1	01	-1	1	LSB
			2, 3		-1.5	1.5	
	$+PSS_2$	11.4 V ≤ V_{CC} ≤ 12.6 V, Output transition = 11111111111X - 00000000000X 4/	1	01	-1	1	LSB
Power supply sensitivity to V_{LOGIC}	$+PSS_3$	4.5 V ≤ V_{LOGIC} ≤ 5.5 V, Output transition = 11111111111X - 00000000000X 4/	1, 2, 3	01	-0.5	0.5	LSB
Power supply sensitivity to V_{EE}	$-PSS_1$	-16.5 V ≤ V_{EE} ≤ -13.5 V, Output transition = 11111111111X - 00000000000X 4/	1	01	-1	1	LSB
			2, 3		-2	2	
	$-PSS_2$	-12.6 V ≤ V_{EE} ≤ -11.4 V, Output transition = 11111111111X - 00000000000X 4/	1	01	-1	1	LSB
Unipolar offset voltage	V_{IO}	Output transition = 00000000000X 4/	1	01	-2	2	LSB
			2, 3		-3	3	
Bipolar zero	BZ	Output transition = XXXXXXXXXXX, bipolar, VFSR = 20 V 4/	1	01	-4	4	LSB
			2, 3		-6	6	
Gain error	A_E	Output transition = 00000000000X to 11111111111X 4/	1	01	-0.3	0.3	% of FSR
			2, 3		-0.55	0.55	
	BPA_E	Bipolar, VFSR = 20 V 4/	1		-0.3	0.3	% of FSR
			2, 3		-0.55	0.55	
Integral linearity error	L_E	Abbreviated test, Bipolar mode 20 V range 4/	1	01	-1/2	1/2	LSB
			2, 3		-1	1	
Differential linearity error	DL_E	Abbreviated test, Bipolar mode 20 V range 4/	1, 2, 3	01	-1	1	LSB

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Input resistance	$R_{IN}10V$	10 V span input	1	01	3.75	6.25	kΩ
			2, 3		3	7	
	$R_{IN}20V$	20 V span input	1		7.50	12.50	kΩ
			2, 3		6	14	
Unipolar offset voltage drift	dV_{IO}/dT	Output transition = 00000000000X 4/	2, 3	01	-1	1	LSB
Bipolar zero drift	dB_Z/dT	Output transition = XXXXXXXXXXX, bipolar, VFSR = 20 V 4/	2, 3	01	-2	2	LSB
Gain error drift	dA_E/dT	Output transition = 00000000000X to 11111111111X 4/	2, 3	01	-10	10	LSB
	$\frac{dBPA_E}{dT}$	Bipolar, VFSR = 20 V 4/	2, 3	01	-10	10	LSB
Functional tests		See 4.4.1c	7, 8	01			
Conversion time 5/	t_C	VIN = -1 V max. Output code = 000000000000, 8 bit cycle	9, 10, 11	01		8.5	µs
		VIN = 11 V max. Output code = 111111111111, 12 bit cycle	9, 10, 11			11	µs
STS delay from $R/\overline{C}$ 2/ 5/	t_{DS}	Low to high transition, referenced to high to low $R/\overline{C}$ transition. Output code = 000000000000	9	01		200	ns
Low $R/\overline{C}$ pulse width 2/ 5/	t_{HRL}	Minimum $R/\overline{C}$ pulse width required to start a conversion	9	01	50		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid after R/$\overline{C}$ low 2/ 5/	t_{HDR}	Output data valid, referenced to high to low R/$\overline{C}$ transition, Output code = 000000000000 & 111111111111	9	01	25		ns
STS delay after data valid 2/ 5/	t_{HS}	STS high to low, transition referenced to valid output data, Output code = 000000000000 & 111111111111	9	01		300	ns
High R/$\overline{C}$ pulse width 2/ 5/	t_{HRH}	Minimum R/$\overline{C}$ pulse width required to enable output bits, Output code = 000000000000 & 111111111111	9	01	150		ns
Data access time 2/ 5/	t_{DDR}	Output data valid, referenced to low to high R/$\overline{C}$ transition, Output code = 000000000000 & 111111111111	9	01		150	ns
STS delay from CE 2/ 5/	t_{DSC}	Low to high transition, referenced to low to high CE transition, Output code = 000000000000	9	01		200	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
CE pulse width 2/ 5/	t_{HEC}	Minimum CE pulse width required to start a conversion	9	01	50		ns
$\overline{CS}$ to CE setup 2/ 5/	t_{SSC}	Minimum time required from a high to low $\overline{CS}$. Transition to low to high CE transition for a conversion to start from CE	9	01	50		ns
$\overline{CS}$ low during CE high 2/ 5/	t_{HSC}	Minimum time required from a low to high CE. Transition to low to high $\overline{CS}$ transition for a conversion to start	9	01	50		ns
R/$\overline{C}$ to CE set up 2/ 5/	t_{SRC}	Minimum time required from a high to low R/$\overline{C}$. Transition to low to high CE transition for a conversion to start from CE	9	01	50		ns
R/$\overline{C}$ low during CE high 2/ 5/	t_{HRC}	Minimum time required from a low to high CE. Transition to low to high R/$\overline{C}$ transition for a conversion to start	9	01	50		ns
A_0 to CE set up 2/ 5/	t_{SAC}	Minimum time required from a low to high or high to low A_0. Transition to low to high CE. Transition to initiate an 8-bit or 12-bit conversion, respectively	9	01	0		ns
A_0 valid during CE high 2/ 5/	t_{HAC}	Minimum time required from a low to high CE. Transition to low to high or high to low A_0 transition to guarantee a 12-bit or 8-bit conversion, respectively	9	01	50		ns
Access time from CE 2/ 5/	t_{DD}	Output data valid, referenced to low to high CE transition, Output code = 000000000000 & 111111111111	9	01		150	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Data valid after CE low 2/ 5/	t_{HD}	Output data valid, referenced to high to low CE transition, Output code = 000000000000 & 111111111111	9	01	25		ns
Output float delay 2/ 5/	t_{HL}	Output delay to HI-Z, referenced to high to low CE transition, Output code = 000000000000 & 111111111111	9	01		150	ns
$\overline{CS}$ to CE setup 2/ 5/	t_{SSR}	Minimum time from $\overline{CS}$ high to low transition to CE low to high transition to guarantee data valid is controlled by CE, Output code = 000000000000 & 111111111111	9	01	50		ns
R/$\overline{C}$ to CE setup 2/ 5/	t_{SRR}	Minimum time from R/$\overline{C}$ low to high transition to CE low to high transition to guarantee data valid is controlled by CE, Output code = 000000000000 & 111111111111	9	01	0		ns
A_0 to CE setup 2/ 5/	t_{SAR}	Minimum time from A_0 high to low or low to high transition to CE low to high transition to guarantee the correct byte gets enabled.	9	01	50		ns
$\overline{CS}$ valid after CE low 2/ 5/	t_{HSR}	Minimum time from CE high to low transition to $\overline{CS}$ low to high transition to guarantee high impedance state is controlled by CE.	9	01	0		ns
R/$\overline{C}$ high after CE low 2/ 5/	t_{HRR}	Minimum time from CE high to low transition to R/$\overline{C}$ high to low transition to guarantee device will disable before another conversion is initiated.	9	01	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
A_0 valid after CE low 2/ 5/	t_{HAR}	Minimum time from CE high to low transition to A_0 high to low or low to high transition to guarantee enabled byte does not change until device is disabled.	9	01	50		ns

1/ V_{CC} = +15 V, V_{EE} = -15 V, V_{LOGIC} = 5.0 V, 10 V input range only.

2/ If not tested, shall be guaranteed to the limits specified in table I herein.

3/ $P_D = (V_{CC} \times I_{CC} + V_{EE} \times I_{EE} + V_{LOGIC} \times I_{LOGIC})$. Power dissipation shall be calculated using the two output code conditions 0000 0000 0000 and 1111 1111 1111.

4/ X represents the transition point between adjacent code words.

5/ See figure 4.

Device type	01
Case outline	X
Terminal number	Terminal symbol
1	V_{LOGIC}
2	12/ 8
3	CS
4	A_0
5	R/C
6	CE
7	V_{CC}
8	REF OUT
9	AC
10	REF IN
11	V_{EE}
12	BIP OFF
13	10 V INPUT
14	20 V INPUT
15	DC
16	DB0(LSB)
17	DB1
18	DB2
19	DB3
20	DB4
21	DB5
22	DB6
23	DB7
24	DB8
25	DB9
26	DB10
27	DB11(MSB)
28	STS

FIGURE 1. Terminal connections.

CE	$\overline{CS}$	R/$\overline{C}$	12/$\overline{8}$	A_O	OPERATION
0	X	X	X	X	None
X	1	X	X	X	None
↑	0	0	X	0	Initiate 12-bit conversion
↑	0	0	X	1	Initiate 8-bit conversion
1	↓	0	X	0	Initiate 12-bit conversion
1	↓	0	X	1	Initiate 8-bit conversion
1	0	↓	X	0	Initiate 12-bit conversion
1	0	↓	X	1	Initiate 8-bit conversion
1	0	1	1	X	Enable 12-bit output
1	0	1	0	0	Enable 8 MSBs only
1	0	1	0	1	Enable 4 LSBs plus 4 trailing zeroes

FIGURE 2. Truth table.

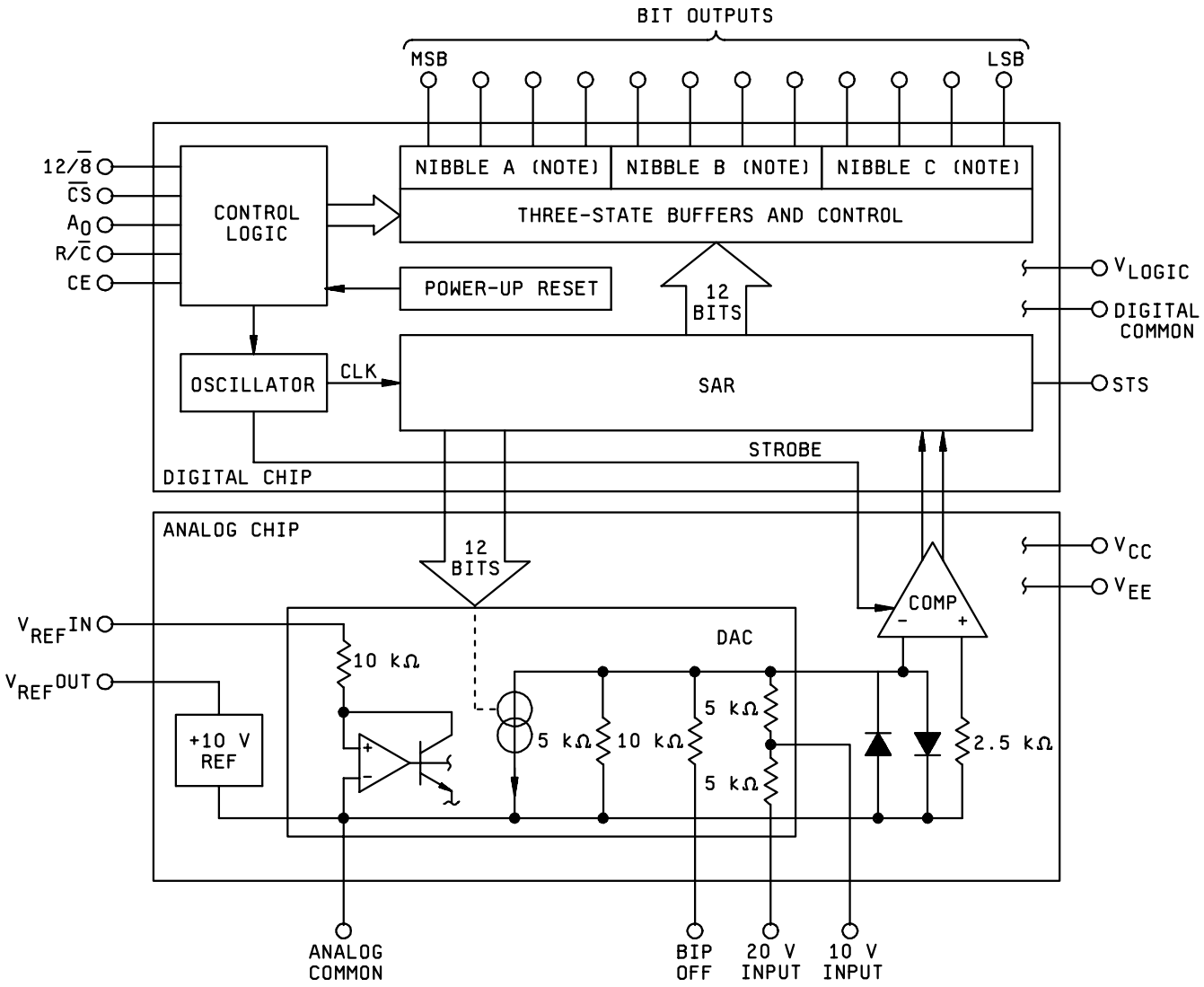


FIGURE 3. Block diagram.

CONVERT START TIMING

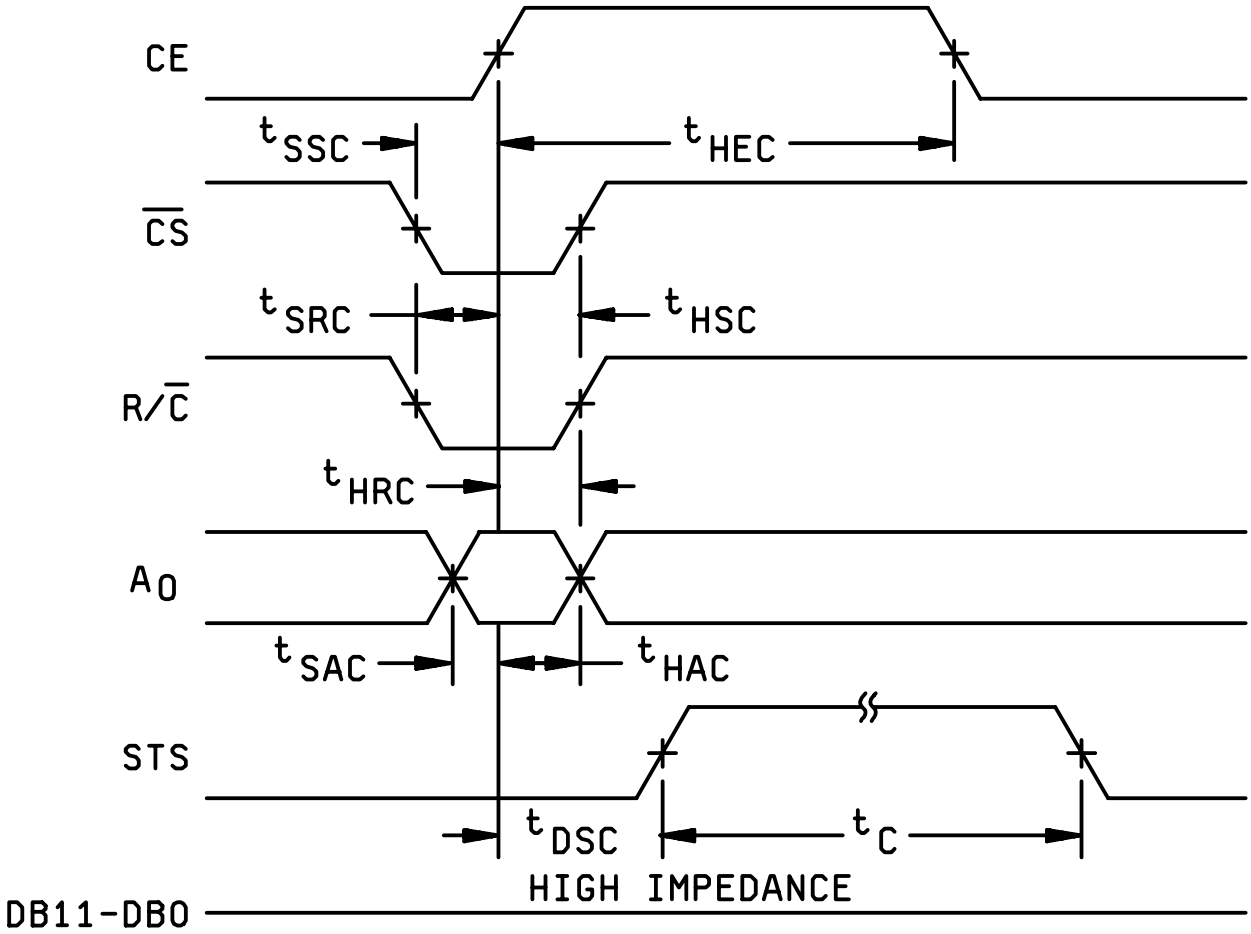


FIGURE 4. Timing waveforms.

READ CYCLE TIMING

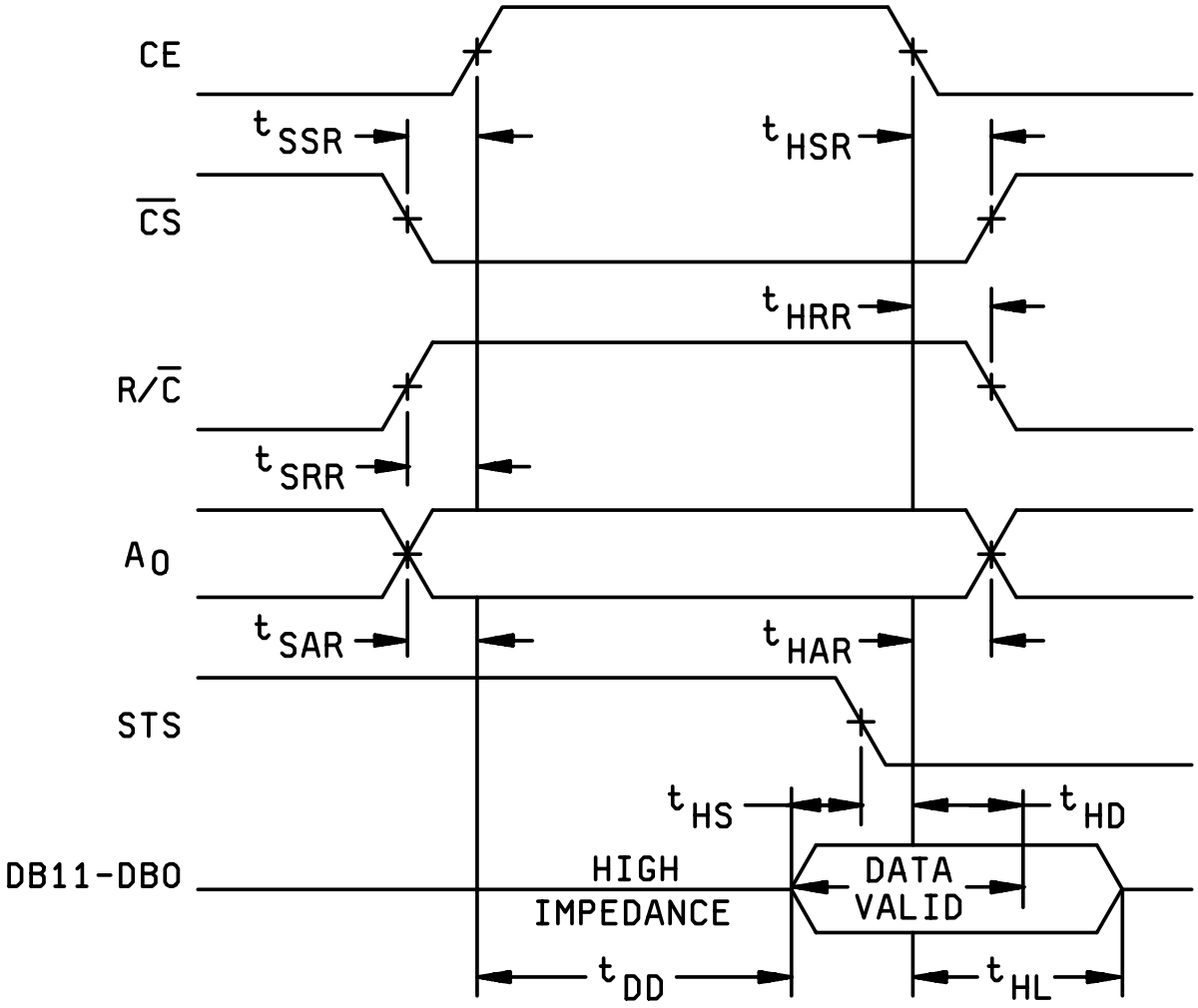


FIGURE 4. Timing waveforms - Continued.

LOW PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED AFTER CONVERSION

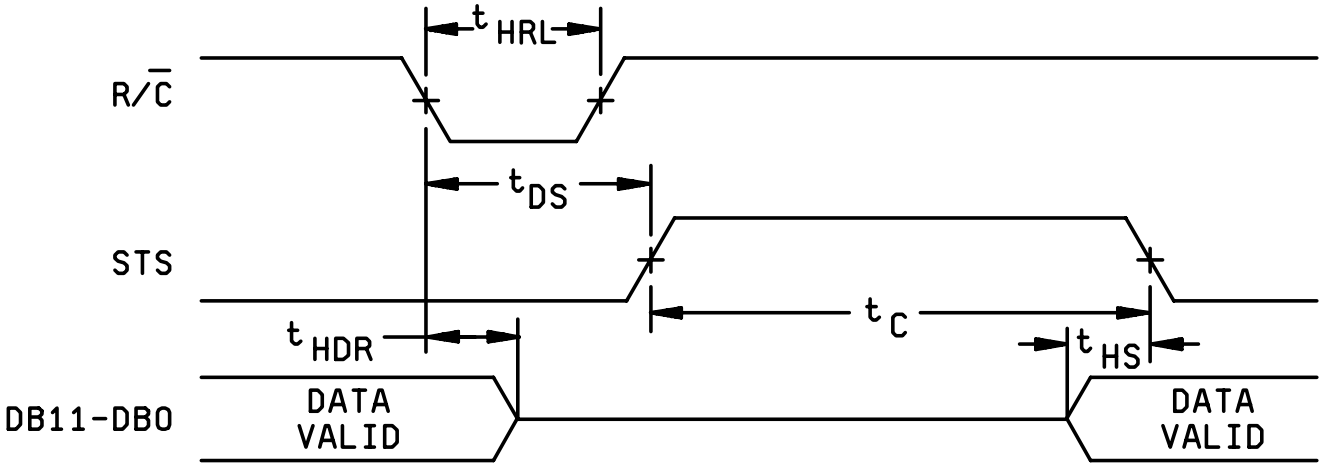


FIGURE 4. Timing waveforms - Continued.

HIGH PULSE FOR R/$\overline{C}$ - OUTPUTS ENABLED WHILE R/$\overline{C}$ HIGH, OTHERWISE HIGH-Z

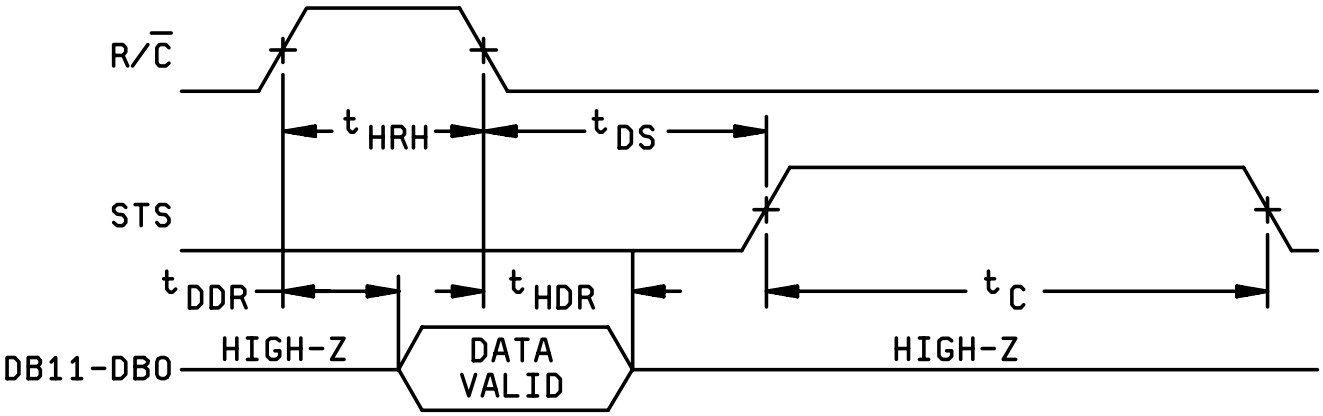


FIGURE 4. Timing waveforms - Continued.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 93 (see MIL-PRF-38535, appendix A).

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B or as modified in the device manufacturer's quality management (QM) plan.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	1	1
Final electrical parameters (see 4.2)	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 1/	1,2,3,7,8, 9,10,11 2/
Group A test requirements (see 4.4)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11
Group C end-point electrical parameters (see 4.4)	1	1	1,2,3,7,8, 9,10,11
Group D end-point electrical parameters (see 4.4)	1	1	1
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. Subgroups 4, 5 and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0547.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

V_{LOGIC}	Logic supply
12/$\overline{8}$	Data mode select
$\overline{CS}$	Chip select
A_O	Byte address/short cycle
R/$\overline{C}$	Read/convert
CE	Chip enable
V_{CC}	Positive supply
REF OUT	Reference output
AC	Analog common
REF IN	Reference input
V_{EE}	Negative supply
BIP OFF	Bipolar offset
DC	Digital common
STS	Status bit

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 02-07-11

Approved sources of supply for SMD 5962-99582 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9958201QXC	34371	HI1-774T/883

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
34371	Intersil 2401 Palm Bay Blvd P.O. Box 883 Melbourne, FL 32902-0883